

75 Moss St. Apt. 14
San Francisco, CA 94103

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OBJECTIVE

To find a position in a team of highly-motivated engineers developing market-focused electronic products as either a senior engineer or technical lead.

SKILLS

- **Hardware Design** - Schematic capture with OrCAD and ViewLogic, PCB layout review in PADS and PCAD, PCB fab & assembly management, board bring-up and debug in lab
- **Logic Design & Verification** - VHDL, Verilog, Xilinx, Altera, QuickLogic devices, ISE, Synplify, Quartus, Max+Plus, Modelsim, VCS, Aldec simulators, System Generator
- **Software Development** - ANSI C, GNU tool chain, TCL, PERL, shell scripting, TI C6000, ARM7, PowerPC, and M68K assembly
- **Packages and Platforms** - Matlab/Simulink, Microsoft Office products, Windows 98/NT/2000/XP, Linux, FreeBSD, OS X

EXPERIENCE

Hardware Engineer: Xilinx – San Jose, CA (November 2005 – Present)

- Technical Lead - Spartan-3A DSP Video Starter Kit (VSK)
 - VSK includes FPGA base board, video I/O card, and camera PCB hardware designs, four FPGA reference designs (including firmware), and tools.
 - Lead development team consisting of internal and external engineering resources.
 - PCB hardware responsibilities included product definition, specification, component selection, design review, debug, validation, review of manufacturing test procedures, and coordination with chip manufacturers.
 - Wrote initial HDL for video timing detector and generator as well as modifications to frame writer and display controller to support new memory controller.
 - Developed CMOS camera reference design including Bayer filter, video frame buffer, DVI display capability, and video recording to CompactFlash.
 - Implemented camera processing IP to remove stuck pixels using median filter.
 - Developed system-level test methods for camera, DVI, and S-Video reference designs.
 - Implemented architectural improvements on firmware driver and library APIs in order to improve usability and integration with tools.
 - Coordinated tools teams to make sure hardware and reference designs are properly supported.
 - Provided guidance to improve company design practices including: development of standardized video bus interface for video IP as well as standardized interfaces for all IP.
- Senior Engineer – Co-Processing / Virtual Socket Adapter
 - Contributed to definition of co-processing methodology for System Generator.
 - Developed Board Support Package for Video Co-processing Kit including automated generation of bus interface IP, address mapping, and interrupt logic.
 - Provided engineering guidance on definition and development of next-generation co-processing kits.
 - Supported marketing with various co-processing projects outsourced to 3rd party developers.

Principal/Owner: Integral Point – San Francisco, CA (December 2001 – October 2005)

Over 15 designs were delivered to clients ranging from startup to Fortune 500. Responsibilities ranged from full project management to engineering contributor. All hardware and FPGA designs were architected, implemented, verified, tested, and integrated with customer equipment. Hardware designs also included prototype builds, BOM management, and development of manufacturing test procedures.

- Hardware Designs
 - Hard disk storage co-processor module including TI 6415 DSP, Xilinx Virtex-II Pro FPGA, and Serial ATA host controller.
 - PCI Mezzanine Card (PMC) including Xilinx Virtex-II Pro FPGA and two 1GHz TI 6416T DSPs.
 - PCI Mezzanine Card (PMC) including largest Xilinx Virtex-II Pro FPGA, and DDR2 memory.
- FPGA Designs
 - Beam Steering Controller Hub utilizing Xilinx Virtex-E FPGA included dual interfaces to CCD video sensor boards, SerDes, packet routing, TI DSP interface, RS-232 and RS-422 UARTs, ADC/DAC interfaces.

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Later work involved porting this design to a Virtex II device and adding of video feature analysis capabilities.

- Multiple designs for laser wavelength control system using Altera FLEX6000 and PowerPC processor modified to add 12bit video interface to CCD sensor board, 10Mbit SPI port and ZBT memory controller.
- Communication interface to laser power amplifier control system using Spartan-II FPGA included four 10Mbit SPI transceivers communicating with PLX 9030 PCI bridge.
- Trigger generator for laser power amplifier control using Spartan-II FPGA converted from single channel triggering to dual channel, interfaced via PLX 9030 PCI bridge.
- Hard disk storage co-processor module logic design using Xilinx Virtex-II Pro included TI DSP interface, high-speed digital bus, communication ports, and PCI interface.
- Multi-purpose Digital I/O module implemented in Altera 10K FPGA included stepper motor driver, UART interface, Motorola 68K processor interface, SerDes, as well as proprietary interfaces.
- Firmware Development
 - Developed variety of firmware test applications to exercise Beam Steering Controller Hub logic design. This code included bit error rate testing (BERT) using pseudo random binary sequences (PRBS).
 - Developed boot code in assembly for TI DSP on hard disk storage co-processor module and assisted in development of driver for Serial ATA host controller.
 - Ported proprietary RTOS from Motorola 68K assembly to ANSI C for use with TI DSP including flash boot-loader.
 - Developed manufacturing test code for PMC modules including PCI bus exerciser.

Design Engineer: Gordian – Santa Ana Heights, CA (May 2000 to August 2001)

- IQinVision iQeye3
 - Hardware design for network camera including design of a DSP daughter board for real-time video compression.
 - Two CMOS image sensor boards were developed: one with megapixel resolution and one 3 megapixels which used an external high-speed ADC.
 - Firmware for camera image correction including fixed-pattern noise and stuck pixel removal was developed.
 - Auto-gain algorithms were developed to support image sensor hardware.
- AudioRamp iRad-N
 - Developed audio driver for handling transfer of compressed audio data from network, decoding, and playback in real-time.
 - Audio codec work included ADPCM and MP3 decoding as well as sample-rate conversion.
 - Low-level enablement of caches and hardware memory protection was completed as well as development of boot code in ARM assembly.
- uCLinux
 - Ported Linux to an internally-developed M68K platform.

EDUCATION

- University of California – Santa Barbara, CA
 - B.S. Electrical Engineering
 - Relevant coursework: digital design methodologies, computer architecture, digital signal processing.
- University of California – Santa Cruz, CA
 - Continuing Education
 - Coursework: SystemVerilog Verification
- University of California – Irvine, CA
 - Continuing Education
 - Coursework: Product Management

CERTIFICATIONS

- California Department of Consumer Affairs Engineer In Training (EIT) – Cert. #116945
- IPC – Certified Interconnect Designer

REFERENCES

Available upon request

2000

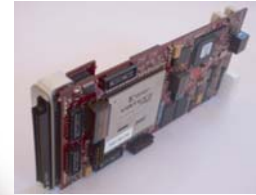


iRad-N MP3 Player

Dual DSP PMC



2005



High-Capacity FPGA PMC



2006

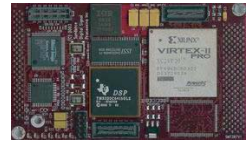


Power Amplifier Controller
Wavelength Controller

2001



iQeye3 Camera



Disk Storage Module



2007



Video Co-Processing Kit



2002

2004



Beam Steering Controller

2003

Spartan-3A DSP Video Starter Kit



2008